

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 62-023170

(43)Date of publication of application : 31.01.1987

(51)Int.Cl.

H01L 29/78

H01L 29/08

H01L 29/52

(21)Application number : 60-163346

(71)Applicant : NEC CORP

(22)Date of filing : 23.07.1985

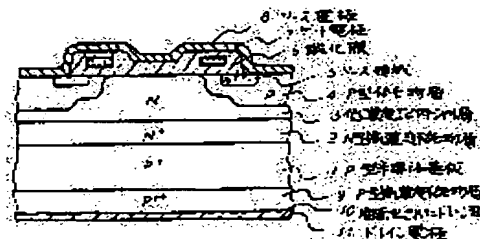
(72)Inventor : USUNAGA YUKIYASU

## (54) MANUFACTURE OF VERTICAL TYPE FIELD-EFFECT TRANSISTOR FOR POWER

## (57)Abstract:

**PURPOSE:** To improve an ohmic contact on the drain side, and to increase withstanding voltage and lower ON resistance while enhancing productivity by forming a high-concentration impurity layer having a different conduction type to semiconductor substrate itself through an ion implantation method or a hot gas diffusion method.

**CONSTITUTION:** An N-type high-concentration impurity layer 2 is shaped to a P-type semiconductor substrate 1 through a thermal diffusion method or an ion implantation method, a low-concentration epitaxial layer is formed, a P-type high-concentration impurity layer 9 is shaped on another surface of the P-type semiconductor substrate, and source and gate regions, a P-type impurity layer 4, an N-type impurity layer 5, an oxide film 6 gate electrodes 7 and a source electrode 8 are formed to the epitaxial layer in a self-alignment manner. The surface of the P-type high-concentration impurity layer 9 is roughened, and a roughened drain surface 10 and a drain electrode 11 are shaped.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

BEST AVAILABLE COPY